REMARKS

Claims 1-7 are pending in this application. By this Amendment, claims 2 and 3 are amended for clarification purposes only. Reconsideration in view of the above amendments and following remarks is respectfully requested.

The Office Action rejects claims 2-4 under 35 U.S.C. §112, second paragraph. Claims 2 and 3 are amended to obviate the rejection. Accordingly, it is requested that the rejection under 35 U.S.C. §112, second paragraph, be withdrawn.

The Office Action rejects claims 1-3 and 5 under 35 U.S.C. §103(a) as being unpatentable over Cherne (U.S. Statutory Invention Registration H1435) in view of Hisamoto (U.S. Patent No. 5,115,289); claims 6 and 7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cherne in view of Hisamoto and Yamazaki (U.S. Patent No. 5,959,313). The rejections are respectfully traversed.

In particular, neither Cherne, Hisamoto or Yamazaki, either alone or in combination, disclose or suggest a thin film transistor, including at least an extension of the gate electrode extending outwardly above the channel region, as recited in independent claim 1.

Furthermore, neither Cherne, Hisamoto or Yamazaki, either alone or in combination, disclose or suggest a thin film transistor, including at least an extension extending from at least one end of the gate electrode along a channel length direction, as recited in independent claim 2.

Specifically, Cherne discloses in Fig. 3 body/channel portions or extensions that extend beyond the source and drain regions to provide a body tie access location and, being more heavily doped that the body/channel portions, serve as a channel stop against sidewall parasitic transistor action between the source and drain regions. See col. 1, lines 7-19. As shown in Fig. 3, the extensions are part of the channel region and not part of the gate layer 21.

Hisamoto discloses in Figs. 2c and 2d source wiring 40' and a polycrystalline silicon layer 30' which becomes the gate electrode.

Yamazaki discloses using thin film transistors in a display device as a driving circuit and using that display device in an electronic apparatus.

In contrast to the claimed invention, neither Cherne, Hisamoto or Yamazaki disclose or suggest a thin film transistor, including at least an extension of the gate electrode extending outwardly above the channel region. Furthermore, none of the applied references disclose or suggest at least an extension extending from at least one end of the gate electrode along a channel length direction.

Thus, the applied references would not have resulted in enlarging a side area of the gate electrode in order to improve a heat radiation efficiency of the TFT because Cherne instead extends a body/channel region to act as a channel stop against sidewall parasitic transistor action between the source and drain regions.

Because any combination of the applied references would not have resulted in the gate electrode extensions in claims 1 and 2, it would not have been obvious to combine the applied references to arrive at the claimed invention. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-7 are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' attorney at the telephone number listed below.

Respectfully submitted,

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